**IN THE SPECIFICATION:**

Please replace the paragraph beginning at line 15 of page 1 with the following amended paragraph:

--In general, as the integration level of semiconductor devices, the contact area becomes narrow. As the contact ~~are~~ area is narrowed, there is a problem that the contact resistance is increased due to defective contact. Therefore, in order to confirm that the contact resistance suitable for the semiconductor device before an actual process for manufacturing the device is performed, a test pattern for measuring a contact resistance is manufactured depending on a design rule of a contact actually applied to a device and the contact resistance is measured using the manufactured test pattern for measuring a contact resistance.--

Please replace the paragraph beginning at line 2 of page 2 with the following amended paragraph:

--Referring now to Fig. 1, a plurality of device isolation ~~films~~ structures **12** are formed in a test wafer **11** to define a plurality of active regions. After word lines (not shown) are formed, a plurality of source/drain diffusion layers **13** are formed by source/drain ion implantation process. An interlayer insulating film (not shown) and a contact hole (not shown) are formed on the entire structure in which the plurality of the source/drain diffusion layers **13** are formed. A contact pattern **14** is formed within the contact hole. Two contact patterns **14** are formed in every source/drain diffusion layer **13**. Then, an interconnection pattern **15** for electrically connecting the plurality of the source/drain diffusion layers **13** is formed.--

Please replace the paragraph beginning at line 19 of page 3 with the following amended paragraph:

--A flash EEPROM as a semiconductor device using the self-aligned line contact will be below described as an example. A plurality of device isolation ~~films~~ structures are first formed to define a plurality of active regions. Word lines surrounded by a spacer insulating film are then formed and a source/drain diffusion layer is formed. Next, an interlayer insulating film is then deposited and flattened. A self-aligned contact hole through which the plurality of the source diffusion layers are exposed is formed by a self-aligned source contact process and the self-aligned contact is filled with a conductive layer to form a source line contact.--

Please replace the paragraph beginning at line 22 of page 4 with the following amended paragraph:

--In order to accomplish the above object, a test pattern for measuring a contact resistance according to the present invention, is characterized in that it comprises a test wafer in which a plurality of device isolation ~~films~~ structures are formed to define a plurality of active regions; a plurality of interconnection diffusion layer formed in a word line region crossing the plurality of the device isolation ~~films~~ structures and the plurality of the active regions; a plurality of source diffusion layers formed in a first line contact region located at one side of the word line region; a plurality of source diffusion layers formed in a second line contact region located at the other side of the word line region; and a plurality of line contact pattern formed in the first and second line contact regions, wherein the line contact pattern formed in the first line contact region and the line contact

pattern formed in the second line contact region are alternately positioned and wherein current for measuring a resistance flows along the first line contact region and the second line contact region between the word line in a three-dimensional manner.--

Please replace the paragraph beginning at line 13 of page 5 with the following amended paragraph:

--A method of manufacturing a test pattern for measuring a contact resistance according to the present invention, is characterized in that it comprises the steps of forming a plurality of device isolation ~~films~~ structures in a test ~~wager~~ wafer to define a plurality of active regions; performing an impurity ion implantation process to simultaneously form a source diffusion layer in a plurality of active regions of a first line contact region, an interconnection diffusion layer in a plurality of active regions of a word line and a source diffusion layer in a plurality of active regions of a second line contact region; forming a word line surrounded by an insulating film spacer in the word line region; forming an insulating layer the surface of which is flattened on the entire structure including the word line; forming a self-aligned contact mask on the insulating layer; and forming a plurality of line contact patterns in the first and second line contact regions through a self-aligned contact process using the self-aligned contact mask, wherein the line contact pattern formed in the first line contact region and the line contact pattern formed in the second line contact region are alternately positioned and current for measuring a resistance flows along the first line contact region and the second line contact region between the word line in a three-dimensional manner.--

Please replace the paragraph beginning at line 7 of page 6 with the following amended paragraph:

--Further, a method of manufacturing a test pattern for measuring a contact resistance according to the present invention, is characterized in that it comprises the steps of forming a plurality of device isolation ~~films~~ structures in a test wafer to define a plurality of active regions; performing a ~~threshold voltage~~ ion implantation process to form a threshold voltage ion implantation region in the plurality of the active regions in a word line region; forming a word line in the word line region to form a channel for controlling a threshold voltage; performing an impurity ion implantation process to form a source diffusion layer in each of the plurality of the active regions of a first line contact region and a source diffusion layer in each of the plurality of the active regions of a second line contact region; forming an insulating film spacer surrounding the word line; forming an insulating layer the surface of which is flattened on the entire structure including the word line; forming a self-aligned contact mask on the insulating layer; and forming a plurality of line contact patterns in the first and second line contact regions through a self-aligned contact process using the self-aligned contact mask, wherein the line contact pattern formed in the first line contact region and the line contact pattern formed in the second line contact region are alternately positioned and current for measuring a resistance flows along the first line contact region and the second line contact region between the word line in a three-dimensional manner.--

Please replace the paragraph beginning at line 1 of page 8 with the following amended paragraph:

--As can be seen from Fig. 2, the test pattern for measuring a contact resistance of the present invention includes a plurality of device isolation ~~films~~ structures **30** on a test wafer **20** to define a plurality of active regions **40**; a plurality of interconnection diffusion layers **61a**, **61b** or **61c** in word line regions **60** crossing the plurality of the device isolation ~~films~~ structures **30** and a plurality of active regions; a plurality of source diffusion layers **51a**, **51b** and **51c** in a first line contact region **50** located at one side of the word line regions **60**; a plurality of source diffusion layers **71a**, **71b** and **71c** in a second line contact region **70** located at the other side of the word line regions **60**; a plurality of line contact patterns **500a** and **500b** in the first line contact region **50**; and a plurality of line contact patterns **700a** and **700b** in the second line contact region **70**. A current path **567** is constructed to form a three-dimensional flow of current including the first line contact pattern **500a** in the first line contact region **50**, a first source diffusion layer **51** in the first line contact region **50**, the interconnection diffusion layer **61a** in the word line region **60**, the first source diffusion layer **71a** in the second line contact region **70**, a first line contact pattern **700a** in the second line contact region **70**, and the second source diffusion layer **71b** in the second line contact region **70**.--

Please replace the paragraph beginning at line 23 of page 9 with the following amended paragraph:

--Referring now to Fig. 3, the plurality of the device isolation ~~films~~ structures **30** are formed in the test wafer **20** to define the plurality of active regions **40**. The first line contact region **50** and the second line contact region **70** are defined so that a pair of the line contact regions can be formed between the word line region **60**. An impurity implantation process is implemented to form the source diffusion layers **51a**, **51b** and **51c** in each of the plurality of the active regions **40** of the first line contact region **50**, the interconnection diffusion layers **61a**, **61b** and **61c** in each of the plurality of the active regions **40** of the word line region **60** and the source diffusion layers **71a**, **71b** and **71c** in each of the plurality of the active region **40** of the second line contact region **70**, at the same time.--

Please replace the paragraph beginning at line 2 of page 11 with the following amended paragraph:

--In the above, the self-aligned contact mask **100** is formed to cover an upper portion of the word line **61**, an upper portion of a portion of the device isolation ~~film~~ structure **30** between the first source diffusion layer **51a** and the second source diffusion layer **51b** in the first line contact region **50**, and an upper portion of a portion of the device isolation ~~film~~ structure **30** between the second source diffusion layer **71b** and the third source diffusion layer **71c** in the second line contact region **70**.--

Please replace the paragraph beginning at line 5 of page 13 with the following amended paragraph:

--Referring now to Fig. 6, the plurality of the device isolation ~~films~~ structures **30** are formed in the test wafer **20** to define the plurality of the active regions **40**. The first line contact region **50** and the second line contact region **70** are defined so that the line contact region can form a pair between the word line regions **60**. ~~A threshold voltage~~ An ion implantation process is performed to form the threshold voltage ion implantation regions **610a, 610b** and **610c** in each of the active regions **40** in the word line region **60** to form a channel for controlling a threshold voltage.--

Please replace the paragraph beginning at line 12 of page 13 with the following amended paragraph:

--Referring now to Fig. 7, the word line **61** is formed in the word line region **60** in which the plurality of the ~~threshold voltage~~ ion implantation regions **610a, 610b** and **610c** are formed. An impurity ion implantation process is performed to form the source diffusion layers **51a, 51b** and **51c** in each of the plurality of the active regions **40** of the first line contact region **50** and the source diffusion layers **71a, 71b** and **71c** in each of the plurality of the active regions **40** in the second line contact region **70**. Then, the insulating film spacer **80** surrounding the word line **61** is formed by a deposition process of the insulating film and an etch process of the spacer. Next, the insulating layer **90** the surface of which is flattened is formed on the entire structure including the word line **61**. Next, the self-aligned contact mask **100** is formed on the insulating layer **90**.--

Please replace the paragraph beginning at line 24 of page 13 with the following amended paragraph:

-- In the above, the first line contact region **50** and the second line contact region **70** are electrically connected by the plurality of the ~~threshold voltage~~ ion implantation regions **610a**, **610b** and **610c**. More particularly, the first source diffusion layers **51a** and **71a** in the first and second line contact regions **50** and **70** are electrically connected by the first ~~threshold voltage~~ ion implantation region **610a** in the word line region **60**, the second source diffusion layers **51b** and **71b** in the first and second line contact regions **50** and **70** are electrically connected by the second ~~threshold voltage~~ ion implantation region **610b** in the word line region **60**, and the third source diffusion layers **51c** and **71c** in the first and second line contact regions **50** and **70** are electrically connected by the third ~~threshold voltage~~ ion implantation region **610c** in the word line region **60**. In order for them to be electrically connected, a voltage must be applied to the word line **60** to form a channel.--

Please replace the paragraph beginning at line 13 of page 14 with the following amended paragraph:

--The self-aligned contact mask **100** is formed to cover an upper portion of the word line **61**, an upper portion of a portion of the device isolation ~~film~~ structure **30** between the first source diffusion layer **51a** and the second source diffusion layer **51b** in the first line contact region **50**, and an upper portion of a portion of the device isolation ~~film~~ structure **30** between the second source diffusion layer **71b** and the third source diffusion layer **71c** in the second line contact region **70**.--